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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/123,430	Applicant(s) YATES, DONALD L.	
	Examiner Brook Kebede	Art Unit 2823	

-- The MAILING DATE of this communication appears on th cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7,9-15,17,18,20-27,44,52,58 and 61-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,23,52,58,65,66,72 and 73* is/are allowed.

6)☒ Claim(s) *1,6,7,9-12,14,15,17,18,20-22,24-27,44,61-64,67-71 and 74-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6, 7, 9, 14, 17, 18, 20, 24, 26, 44, 61, 68, 75, 76 and 77 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al., (USPAT/5,275,184).

Re claim 1, Nishizawa et al. disclose a method for removing surface contaminants from air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising rapidly removing an upper portion semiconductor processing fluid present in the bath while the wafers are in the bath (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27 and see abstract).

Re claim 6, as applied to claim 1 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the contaminants include silica (see Fig. 2).

Re claim 7, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from wet etching bath comprising: processing the semiconductor wafer in the wet etching bath containing and etching fluid; subsequently rapidly removing a substantial portion of an upper portion of the etching fluid from the wet etching bath to remove surface contaminants form an air/liquid interface of the wet etching bath while retaining the semiconductor wafer in the etching bath and subsequently removing of the wafer from the bath (see Fig. 2 and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

Re claim 9, as applied to claim 7 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the upper portion of the etching fluid is removed by draining a top portion of the etching fluid from wet etching bath (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 14, Nishizawa et al. disclose a method for removing contaminants from an air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath while the wafers are in the bath by rapidly removing a wafer boat containing the semiconductor wafer from the bath to remove the surface contaminants from air/liquid interface (see Fig. 2).

Re claim 17, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid (i.e., an aqueous HF) into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

Re claim 18 as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the semiconductor is a silicon wafer (see abstract)

Re claim 20, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from an upper surface of

the wet etching vessel by draining of the top portion of the etching fluid from the wet etching vessel (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 24, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel by rapidly removing a wafer boat containing the semiconductor wafers from the wet etching vessel (see Fig. 2).

Re claim 26, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from the upper surface of the wet etching vessel by physically removing a top portion of the etching fluid from the wet etching bath (see Fig. 2).

Re claim 44, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: immersing a wafer boat in an etching vessel having an etching fluid (i.e., an aqueous HF) therein for sufficient time to etch the silicon wafer; and rapidly removing the wafer boat from the etching vessel to remover the contaminants residing on the upper surface of the etching fluid by causing the etching fluid to spill out of the vessel fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

Re claim 61, Nishizawa et al. disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath, to permit flow of said upper portion of

said processing fluid and thereby break eddy currents holding said surface contaminants at said air/liquid interface (see Fig. 2).

Re claim 68, Nishizawa et al. disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in said bath, to permit flow of said upper portion of said processing fluid and thereby while said wafers are in said bath, to break surface tension forces holding said surface contaminants at said air/liquid interface (see Fig. 2).

Re claim 75, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising: processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from said wet etching bath, said act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2).

Re claim 76, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said wet etching bath, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said

air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2).

Re claim 77, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer, said method comprising: processing said semiconductor wafer in a static etching bath containing an etching fluid; and rapidly removing an upper portion of said etching fluid while said semiconductor wafer is in said static etching bath (see Fig. 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10, 27, 62, and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Itoh et al., USPAT/5,795,401.

Re claim 10, Nishizawa et al. teach all the limitation in the claimed limitations, as applied in claim 7, except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 27, Nishizawa et al. teach all the limitation in the claimed invention, as applied in claim 26, except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 62, as applied to claim 61 above, Nishizawa et al. teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 69, as applied to claim 68 above, Nishizawa et al. teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

5. Claims 11, 21, 63 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Mohindra et al., USPAT/5,958,146.

Re claim 11, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid presented in the bath, while the wafer in the bath (see Fig. 2). However, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 21, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid into a wet etching vessel; placing the semiconductor

wafer in the etching fluid; contacting the semiconductor wafer with the etching fluid for a period of time; and rapidly removing a portion of the etching fluid from the upper surface of the wet etching vessel (see Fig. 2). Nishizawa et al. do not specifically mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 63, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitations except the use of valve.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 70, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitations except the use of valve.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

6. Claims 12, 15, 22, 25, 64, 67, 71 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (USPAT/5,275,184) in view of Hayami et al. (USPAT/5,474,616).

Re claim 12, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 15, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath. (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 22, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 25, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid (i.e., an aqueous HF solution) into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel at a non-constant velocity while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath. (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a

hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 64, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitation. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 67, as applied to claim 61 above, Nishizawa et al. disclose all the claimed limitations. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath. (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 71, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitation. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 74, as applied to claim 68 above, Nishizawa et al. disclose all the claimed limitations. However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath. (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Allowable Subject Matter

7. Claims 13, 23, 52, 58, 65, 66, 72 and 73 are allowed over prior art of record.

Response to Arguments

8. Applicants' arguments filed on May 23, 2002 in Paper No. 26 have been fully considered but they are not persuasive.

Regarding claim rejection, i.e., claims 1, 6, 7, 9, 14, 17, 18, 20, 24, 26, 44, 61, 68, 75 – 77, under 35 U.S.C. §102(b), applicants argued that "Nishizawa does not disclose any of the limitations of the claimed invention. Nishizawa discloses an "apparatus for treating a wafer surface" (Col. 3, line 30) and "a system capable of rapidly substituting treatment solutions" (Col. 3, lines 19-20), but not a method for "rapidly removing" an upper portion of the etching fluid containing "surface contaminants," as amended independent claims 1 and 7 recite. Nishizawa is also silent about a method for etching a semiconductor wafer by rapidly removing a portion of said etching fluid from the upper surface of said wet etching vessel," as amended independent claim 17 recites. In Nishizawa, the "old treatment solution inside the container is rapidly

displaced by the new treatment solution" (col. 3, lines 54-55) so that the wafers do not experience contact with air during replacement of the treatment solutions." (Abstract). Applicant expressly notes that Nishizawa does not address "surface contaminants" or "contaminants from an air/liquid interface." As known in the semiconductor art, surface contaminants at the air/liquid interface of a solution are either hydrophobic contaminants, which do not suspend in the solution, or contaminants so light that they float on top of the bath and are trapped in surface tension. Surface contaminants are not contaminants suspended. In a solution but rather contaminants trapped at the surface of that solution. Eddy currents, also called surface currents, and liquid /air surface tension forces trap the surface contaminants at the surface of the bath, making difficult for the removal of such surface contaminants. (Application at 3, lines 7-10). This is why a sudden, physical force is necessary for the removal of the surface contaminants. Simply overflowing a solution, as in Nishizawa, will not suffice for the break of the eddy currents and/or tension forces and the subsequent removal of surface contaminants. Applicant further points out that Nishizawa addresses hydrophilic contaminants or contaminants suspended in a cleaning bath, and not "surface contaminants from an air/liquid interface" in such cleaning bath, as in the claimed invention. In addition, Nishizawa displaces the cleaning solution with a rinsing solution, for example water. Thus, Nishizawa is silent about any "surface contaminants at an air/liquid interface," or about the removal of such surface contaminants which do not suspend in a solution, much less about "'rapidly removing" the upper portion of an upper portion of such solution, as independent claims 1, 7) 17 and 44 recite. In sum, the present invention is not anticipated by Nishizawa."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above.

In response applicants' argument, *Nishizawa discloses an "apparatus for treating a wafer surface" (Col. 3, line 30) and "a system capable of rapidly substituting treatment solutions" (Col. 3, lines 19-20), but not a method for "rapidly removing" an upper portion of the etching fluid containing "surface contaminants," as amended independent claims 1 and 7 recite... Simply overflowing a solution, as in Nishizawa, will not suffice for the break of the eddy currents and/or tension forces and the subsequent removal of surface contaminants. Applicant further points out that Nishizawa addresses* ***hydrophilic contaminants or contaminants suspended*** *in a cleaning bath, and not "****surface contaminants from an air/liquid interface****" in such cleaning bath, as in the claimed invention. In addition, Nishizawa displaces the cleaning solution with a rinsing solution, for example water. Thus, Nishizawa is silent about any "surface contaminants at an air/liquid interface," or about the removal of such surface contaminants which do not suspend in a solution, much less about '"rapidly removing" the upper portion of an upper portion of such solution, as independent claims 1, 7) 17 and 44 recite*, the examiner respectfully submits that Nishizawa et al. '184 disclose a method for rapidly removing an upper portion of the etching fluid cot (see Fig. 2). As shown figure 2, the flow of the solution is rapid.

The instant application does not disclose or claim the flow rate of rapid removal of the solution. In the absence of such disclosure, the claimed limitation is within the scope of the prior art. In addition, Nishizawa et al. disclose the "etching fluid," (i.e., HF solution) containing contaminants and rapidly removing the fluid. In Figure 2, the wafer (W) is immersed in the cleaning (etching) bath and the contaminants were being rapidly removed form etching bath with

the etching solution. The wafer (W) contains the contaminants and when it is placed in the cleaning (etching) bath which contains the cleaning (etching) solution leaves the surface of the wafer and rapidly removed with the cleaning (etching) solution. As applicants well-know it, the contaminants are a very light particulate that can be deposited on the wafer during fabrication process, such as etching patterning and etc., and can be easily removed form the surface. In order for applicants to suggest or argue, Nishizawa et al. '184 do not teach *rapidly removal of an upper portion of the etching fluid containing "surface contaminants,"* applicants need to establish the following evidence or fact: Applicants need to establish, in Nishizawa et al. '184 disclosure, the wafer does not have any contaminant or the density contaminant on the wafer so high so that after removal by the solution it settles in the bottom the cleaning (etching) bath. In the absence of such evidence, applicants argument that Nishizawa et al. '184 do not teach *rapidly removal of an upper portion of the etching fluid containing surface contaminants* is not valid.

In response to applicants argument, *Nishizawa addresses* ***hydrophilic contaminants or contaminants suspended*** *in a cleaning bath, and not* ***"surface contaminants from an air/liquid interface"*** *in such cleaning bath, as in the claimed invention. In addition, Nishizawa displaces the cleaning solution with a rinsing solution, for example water. Thus, Nishizawa is silent about any "surface contaminants at an air/liquid interface," or about the removal of such surface contaminants which do not suspend in a solution, much less about '"rapidly removing" the upper portion of an upper portion of such solution,* the examiner respectfully submits the following:

As of record, the Examiner submits the meaning for the terms ***hydrophilic*** and ***hydrophobic*** which is taken from Merriam Webster's Colligate Dictionary 10th edition in page 568.

Hydrophilic: *relating to, or having strong affinity for water.*

Hydrophobic: *relating to, or suffering from hydrophobia, lacking affinity for water.*

There are two problems with the applicants argument in which *Nishizawa addresses* ***hydrophilic contaminants or contaminants suspended in a cleaning bath****, and not* ***"surface contaminants from an air/liquid interface"*** *in such cleaning bath, as in the claimed invention.* First, Nishizawa et al. '184 disclosure neither teach nor suggest the contaminants are either hydrophilic or hydrophobic. Second, there is no teaching or suggestion of suspension of the contaminants in the cleaning (etching) bath in Nishizawa et al. reference. The Examiner respectfully requests applicants to point the lines and paragraphs to the Office where in Nishizawa et al. reference disclose the teaching or suggestion of ***hydrophilic contaminants or contaminants suspended in a cleaning bath*** can be found. Furthermore, the use of water in Nishizawa et al. disclosure is in order to further rinse the acid solution form the surface of the wafer after the wafer is treated with an acid solution during to removal of the contaminants. In response to applicants' contention, *Nishizawa is silent about any "surface contaminants at an air/liquid interface,"* the Examiner respectfully submits that Nishizawa et al. disclose *air/liquid interface (*see Col. 2, line 61 – Col. 3, lines 23). Nishizawa et al. disclose the method of rapid wafer treatment that utilizes dipping type wafer treatment (i.e., immersing the wafer in treatment bath). As shown in Fig. 2, the top of the treatment bath is an open bath and the liquid is flown over the top and the contaminants are being removed at an air/liquid interference. In order applicants to establish a valid argument, i.e., Nishizawa et al. do not teach removal of *surface contaminants at an air/liquid interface*, applicants should establish a valid evidence that the cleaning (etching) system is a closed system or the contaminants never get over the top of the

etching solution and leave the etching bath due to high density nature or other physical characteristics. The Examiner respectfully submits that Nishizawa et al. disclose removal of surface contaminants at an air/liquid interface either directly or inherently.

In addition before responding to applicants' contention that *simply overflowing a solution, as in Nishizawa, will not suffice for the break of the eddy currents and/or tension forces and the subsequent removal of surface contaminants. Applicant further points out that Nishizawa addresses hydrophilic contaminants or contaminants suspended in a cleaning bath, and not "surface contaminants from an air/liquid interface" in such cleaning bath, as in the claimed invention. In addition, Nishizawa displaces the cleaning solution with a rinsing solution, for example water. Thus, Nishizawa is silent about any "surface contaminants at an air/liquid interface," or about the removal of such surface contaminants which do not suspend in a solution, much less about '"rapidly removing" the upper portion of an upper portion of such solution, as independent claims 1, 7) 17 and 44 recite. In sum, the present invention is not anticipated by Nishizawa,"* the Examiner respectfully submits the interpretation of the ***Eddy (Eddy current***) which is taken from Merriam Webster's Colligate Dictionary 10th edition in page 366.

***Eddy**: a: a current of water or air running contrary to the main current; esp: a circular current: WHIRLPOOL b: something moving similarly 2: a contrary or circular current.*

***Eddy current**: an electric current induced by an alternating magnetic field.*

As a well-known phenomena, in the art of fluid dynamics, Eddy current is the current that flow opposite direction the flow of the fluid (i.e., air or liquid). Such current is created by a turbulence which can cause agitation the fluid or air which makes vortex. In order the applicants

to establish a valid argument, i.e., *Nishizawa, will not suffice for the break of the eddy currents and/or tension forces and the subsequent removal of surface contaminant*, applicants have to provide an evidence that Nishizawa et al. disclosure does not remove the contaminants form the surface of the wafer. If that the case, the Examiner respectfully requests that applicants to provide an evidence to the Office where in the Nishizawa et al. disclosure the contaminants were not removed form the cleaning (etching) bath. The Examiner respectfully submits that Nishizawa et al. teach the breaking of the eddy currents and/or tension forces and the subsequent removal of surface contaminant either directly or inherently. Therefore, the rejection under 35 U.S.C. §102 is deemed proper.

Regarding claim rejection of claims 10, 27, 62 and 69 stand rejected under 35 U.S.C. § 103 (a), applicants argued that "the claimed invention would not have been obvious over Nishizawa in view of Itoh. First, Nishizawa is silent about the rapid removal of "surface contaminants" or of surface contaminants from an air/liquid interface" by opening a valve, hingedly releasing a door, sliding a door, or telescopically collapsing sidewalls of a vessel containing an etching bath. Second, even if Itoh recites using a paddle, Itoh does not refer to the removal of any contaminants from the etching bath, much less to the removal of "surface contaminants from an air/liquid interface." Itoh merely refers to the scrubbing of a wafer surface using a rotary brush while pressure is applied by jetting a fluid on the other surface of the wafer. Third, Itoh does not teach or disclose rapidly removing of a substantial portion of the etching liquid. Itoh does not even mention an etching fluid. Itoh refers only to a wash liquid that is purified water and that comes into contact with a rotary brush that cleans the wafer surface. Thus, there is no teaching or suggestion in either of these two references for the claimed subject

matter. The references are also not combinable in view of the diverse areas involved in each reference. Nishizawa refers to wafer surface treatment by using at least two different solutions. Itoh, on the other hand, refers to the actual physical cleaning and scrubbing of the wafer surface by mechanical means such as a cylindrical rotary brush. It is clear, therefore, that the rejection is based on picking and choosing selected portions of each reference, without regard to the totality of teachings of the references, in an attempt to improperly use hindsight to reconstruct the invention."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Nishizawa et al. '184 and Itoh et al. '401 teach all the claimed limitations as applied in Paragraph 4 herein above. It would have been within the scope of one of ordinary skill in the art to employ the known process or the disclosed prior process for its disclosed intended purpose to achieve removing of the fluid as disclosed in Itoh et al. '401 reference. Further, in response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claims 11, 21, 63 and 70 under 35 U.S.C. § 103 (a) in combination of Nishizawa et al. '184 and Mohindra et al. '146, applicants argued that "Mohindra et al. ("Mohindra") discloses a cleaning technique for a semiconductor wafer that uses a hot or heated liquid in conjunction with a carrier gas which includes a cleaning enhancement substance. Mohindra discloses the use of control valves in the method of cleaning the semiconductor wafers, and the Office Action points out that "it would have been obvious to one ordinary skill in the art ... to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath." (Office Action at 9). However, the control valves in Mohindra are not used for the rapid removal of "surface contaminants from an air/liquid interface" of an upper portion of the etching fluid, as in the claimed invention. Rather, the control valves in Mohindra are used to allow a fluid to enter a filter bank, after the fluid was heated in a heater, and then into a wet processor. (Col. 5, lines 47-48; Col. 6, lines 29-35). Undoubtedly, the control valve. in. this reference merely "meters the carrier gas to the wet processor," and not a processing fluid of an etching bath, as the claimed invention discloses. Further, the control valve in Mohindra is not used to remove any portion of an etching fluid, and surely does not rapidly remove any surface contaminants, as it merely allows passage of a fluid from a filter bank into a processor. Accordingly, there is nothing in the combination of Nishizawa and Mohindra, without the improper use of hindsight reconstruction, to motivate a person of ordinary skills in the art to arrive at the claimed method."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The

combination of Nishizawa et al. '184 and Mohindra et al. '146 teach all the claimed limitations as applied in Paragraph 5 herein above. It would have been within the scope of one of ordinary skill in the art to employ the known process or the disclosed prior process for its disclosed intended purpose to achieve removing of the fluid as disclosed in Mohindra et al. '146 reference. Further, in response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claims 12, 15, 22, 25, 64, 67, 71 under 35 U.S.C. § 103 (a) in combination of Nishizawa et al. '184 and Hayami et al. '616, applicants argued that "Hayami teaches a method for rinsing plate-shaped articles, such as semiconductor wafers, as well as cleaning equipment for the rinsing method.. (Col. 2, lines 40-43). For this, Hayami uses a cleaning bath in which streams are directed upward from orifices of a feed pipe located near the bottom of the cleaning bath. (Col. 6, lines 1-4; Figures 41-42). The diameters of the orifices are adjusted "so that the jetting pressure of the cleaning water at all the orifices are. uniform. " (Col. 6, lines 11 - 14). Most importantly, Hayami specifically notes that "it is necessary to stably maintain a state where a part of the surface of the cleaning water bulges so as to form uniform

streams on the surface of the cleaning water." (Col. 7, fines 13-16). Thus, while these uniform streams which are directed toward the rear and front walls are formed on the surface of the cleaning water, the semiconductor wafers are "gradually brought into the cleaning water." (Col. 14, lines 40-45). The claimed invention would not have been obvious over Nishizawa in view of Hayami. First, both Nishizawa and Hayami are silent about the rapid removal of "surface contaminants" or of "contaminants from an air/liquid interface" by "hingedly releasing a door" or by "telescopically collapsing sidewalls of a vessel," as amended independent claims 12,15 and 25 recite, and independent claim 22 recites."

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Nishizawa et al. '184 and Hayami et al. '616 teach all the claimed limitations as applied in Paragraph 6 herein above. It would have been within the scope of one of ordinary skill in the art to employ the known process or the disclosed prior process for its disclosed intended purpose to achieve removing of the fluid as disclosed in Hayami et al. '616 reference.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
August 8, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800